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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,159	03/30/2001	Sheng Zhao	871.0013USU	8117

29683 7590 12/03/2003

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2189	6

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,159	ZHAO ET AL.	
	Examiner	Art Unit	
	Nimesh G Patel	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because it exceeds 150 words.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-11, and 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Earnest('338).

4. Regarding claim 1, Earnest discloses a programmable buffer circuit for interfacing a CPU to a plurality of channel interfaces comprising of a dual port memory(Figure 3, Block 100), an arbitrator for arbitrating access to the dual port memory(Column 3, Lines 53-54), an address generator for addressing the dual port memory(Column 5, Lines 59-65), and an allocator and control unit for specifying buffer locations for individual channels(Column 3, Lines 3-15).

5. Regarding claim 2, Earnest discloses control unit to be programmable for operating individual ones of channel buffers in FIFO access mode of operation(Column 3, Lines 3-15).

6. Regarding claim 3, Earnest discloses an integrated circuit containing a dual port memory, CPU, and plurality of interface channels (Column 2, Lines 45-50).

7. Regarding claim 5, Earnest discloses an interface channel comprising of a serial data interface(Column 5, Line 3).

8. Regarding claim 6, Earnest discloses an interface channel comprising of a packet data interface(Column 5, Lines 4-6).

9. Regarding claim 7, Earnest discloses plurality of channels comprising of receive and transmit interfaces(Column 4, Lines 56-63) and an allocator comprising registers for specifying the starting address and size for each of the receive and transmit interfaces(Column 3, Lines 3-15).

10. Regarding claim 8, Earnest discloses plurality of channels comprising of receive and transmit interfaces(Column 4, Lines 56-63) and a receive buffer of one channel interface to be a transmit buffer of another channel(Column 4, Lines 20-23).

11. Regarding claim 9, Earnest discloses a dual port memory couple to a CPU data bus and to a channel data bus that serves a plurality of channel interfaces(Figure 2), programming a control unit for specifying individual ones of buffer locations and sizes within a dual port memory for the channel interfaces(Column 3, Lines 3-15), and arbitrating for access to the dual port memory(Column 3, Lines 53-54). Earnest further discloses the generation of dual port memory address depending on what channel interface is currently selected and on the specified buffer location and size for that channel interface(Column 7, Lines 28-48).

12. Regarding claim 10, Earnest discloses control unit to be programmable for operating individual ones of channel buffers in FIFO access mode of operation(Column 3, Lines 3-15).

13. Regarding claim 11, Earnest discloses an integrated circuit containing a dual port memory, CPU, and plurality of interface channels (Column 2, Lines 45-50).

14. Regarding claim 13, Earnest discloses plurality of channels comprising of receive and transmit interfaces(Column 4, Lines 56-63) and specifying the starting address and size for each of the receive and transmit interfaces(Column 3, Lines 3-15).

15. Regarding claim 14, Earnest discloses plurality of channels comprising of receive and transmit interfaces(Column 4, Lines 56-63) and a receive buffer of one channel interface to be a transmit buffer of another channel(Column 4, Lines 20-23).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Earnest in further view of Begur et al.('649).

17. Regarding claim 4, Earnest does not specifically disclose a channel interface as an audio codec. However, Earnest discloses example data interface circuits and discloses other types of data interface controllers also can be used(Column 5, Lines 2-10). Begur discloses a circuit with plurality of interface channels with an audio codec channel(Column 6, Lines 55-60). Therefore it would have been obvious to one of an ordinary skill in the art to include the audio codec of Begur in Earnest's system for the purpose of handling an audio stream that needs to be encoded/decoded.

18. Regarding claim 12, Earnest discloses an interface channel comprising of a packet data interface and a serial data interface(Column 5, Lines 4-6).

Earnest does not specifically disclose a channel interface as an audio codec. However, Earnest discloses example data interface circuits and discloses other types of data interface controllers also can be used(Column 5, Lines 2-10). Begur discloses a circuit with plurality of interface channels with an audio codec channel(Column 6, Lines 55-60). Therefore it would have been obvious to one of an ordinary skill in the art to include the audio codec of Begur in Earnest's system for the purpose of handling an audio stream that needs to be encoded/decoded.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sodos('237, '532) discloses a method and apparatus for transferring data between memory and a plurality of peripheral units through a plurality of data channels.

Alasti et al.('390) discloses a two-port memory to connect a microprocessor bus to multiple peripherals.

Holm et al.('680) discloses a multiple channel data communication buffer having unique space assigned for each channel with fixed arbitration.

Lewis et al.('043) discloses a data transfer control system including a pool memory, consisting of FIFOs that is coupled to plurality of peripheral devices to provide for the transfer of data between the programmatically associated FIFOs and the peripheral devices.

Conley et al.('420) discloses a buffer memory and method for employing an arbiter state machine for control of data transfer between multiple external peripheral devices and the DRAM buffer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Nimesh G Patel
Examiner
Art Unit 2189

NGP
11/26/03
NP

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100